COMPUTER ARCHITECTURE AND PARALLEL PROCESSING

Semester	Subject Code	Category	Lecture Hrs		Theory Hrs		Practical		Credits
			Per week	Per Sem	Per week	Per Sem	Per week	Per Sem	
I		ELECTIVE - 1	6	90	6	90	0	0	5

COURSE OBJECTIVE

- This paper helps us to understand the advanced level of Computer Architecture and Parallel Processing.

COURSE OUTCOME

successful completion of the course, students will be able to

CO Number	CO Statement	Knowledge Level (K1-K4)
CO1	To learn about computer architecture and different types of processing.	K2
CO2	To understand the principles of pipeline processors and vectors processing.	K3
CO3	Implementation of SIMD and associative array processing.	K2
CO4	To learn about the multiprocessor architecture and programming.	K3
CO5	Understanding and Analyzing Multi-process Scheduling Algorithms	K4

Knowledge Level – K1-Remember, K2- Understand, K3-Apply, K4-Analyze

MAPPING WITH PROGRAMME OUTCOME

COS	PO1	PO2	PO3	PO4	PO5	PO6
CO1	S	M	S	S	M	M
CO2	S	S	S	M	S	M
CO3	S	S	M	S	M	M
CO4	S	S	S	M	S	S
CO5	S	M	S	M	S	M

S-Strong, M-Medium and L-Low

UNIT I – COMPUTER ARCHITECTURE INTRODUCTION **18 Hours**

Introduction - Evolution of Computer systems - Trends of Parallel Processing - Parallelism in Uniprocessor Systems - Architecture, Mechanisms, Multiprogramming and Timesharing - Parallel Computer Structures - Pipeline, Array, Multiprocessor, Performance of Parallel computer, Data Flow - Architectural Classification - Applications.

UNIT II – PARALLEL PROCESSING **18 Hours**

An Overlapped Parallelism - Instruction and Arithmetic Pipelines - Principles of Designing Pipeline Processors - Instructions Prefetch and Branch Handling, Data Buffering and Busing Structures – JobSequencing and Collision Prevention - Vector Processing Requirements - Characteristics of Vector Processing, Pipelined Vector Processing Methods.

UNIT III – PROCESSORS **18 Hours**

SIMD Array Processors - SIMD Interconnection Networks - Associative Array Processing.

UNIT IV – MULTIPROCESSOR ARCHITECTURES **18 Hours**

Multiprocessor Architecture and Programming: Functional Structures-InterconnectionNetworks- Parallel Memory Organization.

UNIT V - MULTIPROCESSOR OPERATING SYSTEMS **18 Hours**

Multiprocessor Operating Systems- Interprocessor Communication Mechanisms-Multiprocessor Scheduling Strategies-Parallel Algorithms for Multiprocessors.

Distribution of Marks: Theory 70% and Problem 30%

TEXTBOOKS

S. NO	AUTHORS	TITLE	PUBLISHERS	YEAR OF PUBLICATION
1	Kai Hwang, Faye A. Briggs	Computer Architecture and Parallel Processing	McGraw Hill book company	1985
2	John P. Hayes	Computer Architecture and Organization	MCH	1988

REFERENCEBOOKS

S. NO	AUTHORS	TITLE	PUBLISHERS	YEAR OF PUBLICATION
1	V. Rajaraman, C. Sivaram Murthy	Parallel Computers Architectures and Programming	PHI	2003
2	Michael J. Quinn	Parallel computing theory and practice	Tata McGraw Hill	2002
3	Wilkinson, Michael Allen	Parallel programming: techniques and Applications	Prentice hall	1999

WEB RESOURCES

1. https://www.class-central.com/course/nptel-computer-organization-and-architecture-a-pedagogical-aspect-9824
2. https://www.class-central.com/course/nptel-computer-organization-and-architecture-a-pedagogical-aspect-9824
3. https://www.mooc-list.com/tags/parallel-programming

TEACHING METHODOLOGY

- Class room teaching & Group discussions
- Seminars & Smart Class room
- Chart/Assignment & Simulation Model

SYLLABUS DESIGNERS

- Mrs.G.SANGEETHA LAKSHMI, Assistant professor & HOD, Dept of Computer Science & Applications
- Mrs. S.SHANTHI , Assistant Professor , Dept of Computer Science & Applications